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EXAMINER	
JOSEPH, DENNIS P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 10/524,968	Applicant(s) DE GREEF ET AL.
	Examiner DENNIS P. JOSEPH	Art Unit 2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _05 August 2009_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-11 and 13-20_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-11 and 13-20_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to amendments filed for application No. 10/524,968 on August 5, 2009. Claims 1-11 and 13-20 are pending and have been examined.

Allowable Subject Matter

2. **Claims 17, 19 and 20** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 17, 19 and 20** rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

These claims recite formulae and variables combined in a way which aren't described in the specification. Examiner notes the sections Applicant referenced when claiming there was support, but this is not in enough detail and furthermore, requires one of ordinary skill in the art to make some jumps to see how the formulae make sense or have support. Applicant is also

asked to provide more details on these claims, such as the multiplier coefficients, etc.

Appropriate correction is respectfully required, thank you.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 16, 17, 19 and 20** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

These claims recite a constant value CV. However, this term is not defined in the claim language like some of the other variables. Without a proper definition, it is a vague, indefinite term and it is not defined either in Claim 16. What is it and why is it in the formulae? It doesn't seem to be dependent on other factors, such as the current pixel or a neighboring pixel.

For purposes of examination, it will be interpreted as it being a, respectfully, random value, until it is defined.

Claim Rejections – 35 USC § 103

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 1-3, 5 and 7** rejected under 35 U.S.C. 103(a) as being unpatentable over Van Dalfsen et al. (US 2001/0005186 A1) in view of Kwak et al. (6,166,781), further in view of Zlotnick (US 6,522,784 B1)

Van Dalfsen teaches in Claim 1:

A video circuit for processing video signals which show images on a display panel with linear light transition ([0005]), comprising a gamma correction circuit ([0037]), a quantizer (Figure 3, quantizer 304, [0046]) and a sub-field generator circuit ([0001], Figure 3, 306 and Column 3, Table 1 shows the combinations), but

Van Dalfsen does not explicitly teach that the circuit is "wherein a coarse adjustment of the quantization is made in a first random-access memory and a fine adjustment of the quantization is made in a second random-access memory." He does not teach of a two-stage adjustment process done with LUTs.

However, in the same field of endeavor, display driving methods, Kwak teaches and shows in Figure 7, "After step 106, multiplier 90 multiplies the second data read from second LUT 86

with the lower bits, and outputs the product to adder 88 (step 108). After step 108, adder 88 adds the first data from first LUT 84 to the output from multiplier 90, and outputs the sum to an output port OUT as digital corrected data." (Kwak, Column 9, Lines 12-16) Figure 7 shows the first LUT 84 and the second LUT 86. 86 multiplies and makes a coarse adjustment and the 84 adds and makes a fine adjustment. Furthermore, it is obvious to one of skill in the art that the respective LUTs are associated with the addition and multiplier functions.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate two stage adjustment process as taught by Kwak with Van Dalfsen's display device by implementing the two LUTs to quantize the signal with the motivation that "RAM is typically more complicated and larger than ROM, making look up table size even more critical in programmable systems." (Kwak, Column 1, Lines 65-67) This is important because "Larger look up tables make integration more difficult and increases system costs" (Kwak, Column 1, Lines 61-62) and it also reduces the depth and width of the LUT leading to less output error.

Kwak does not explicitly teach "wherein multiple quantization errors of different neighboring pixels of a current pixel are used to quantize the current pixel." As discussed above, he does teach of making adjustments/quantizing the data as discussed above.

However, using absolute values in comparing the neighboring pixel data to determine the quantization error, QE, of the current pixel, is well known in the art and is commonly used to calculate the QE.

To emphasize, in the same field of endeavor, quantization and compression/reordering of image data, Zlotnick teaches of using quantized images and reordering pixels by value and location and discloses this step in Figure 2. Furthermore, he discloses the absolute difference in position of the pixels values of neighboring pixels is used in the quantization process for rendering the image data, (Zlotnick, Column 6, Lines 1-43)

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the rendering process, as taught by Zlotnick, with Van Dalfsen's correction circuit, as modified by Kwak, with the motivation that by quantizing properly, an efficient compression can be had, reducing the size of the image data, saving space and also allowing for a sharper image, (Zlotnick, Column 1, Lines 50-56)

Van Dalfsen teaches in Claim 2:

A video circuit for processing video signals which display images on a display panel with linear light transition ([0005]), comprising a gamma correction circuit ([0037]), a quantizer (Figure 3, quantizer 304, [0046]) and a sub-field generation circuit ([0001], Figure 3, 306 and Column 3, Table 1 shows the combinations), but

Van Dalfsen does not explicitly teach that the circuit is "wherein most significant bits are quantized in a first random-access memory and least significant bits are quantized in a second random-access memory."

However, in the same field of endeavor, display driving methods, Kwak teaches, "An N-bit digital signal is input via an input port IN. The first LUT 20 stores first data, and reads the stored data using U upper bits (i.e., most significant bits) of the N-bit digital input signal as an address." (Column 5, Lines 3-6) Figure 2 shows the first LUT 20 and this is for the most significant bits., "Multiplier 24 multiplies the M-bit second data, (here, M is varied according to the allowable error) read from the second look up table 22, with the D lower bits (i.e., least significant bits) of the N-bit digital input signal, and outputs the product to adder 26. (Column 5, Lines 21-24) Figure 2 shows second LUT 22. Furthermore, it is obvious to one of skill in the art that the respective LUTs are associated with the addition and multiplier functions.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate two stage bit process as taught by Kwak with Van Dalfsen's display device by implementing the two LUTs to quantize the signal with the motivation that "RAM is typically more complicated and larger than ROM, making look up table size even more critical in programmable systems." (Kwak, Column 1, Lines 65-67) This is important because "Larger look up tables make integration more difficult and increases system costs" (Kwak, Column 1, Lines 61-62) and it also reduces the depth and width of the LUT leading to less output error.

Kwak does not explicitly teach “wherein multiple quantization errors of different neighboring pixels of a current pixel are used to quantize the current pixel.” As discussed above, he does teach of making adjustments/quantizing the data as discussed above.

However, using absolute values in comparing the neighboring pixel data to determine the quantization error, QE, of the current pixel, is well known in the art and is commonly used to calculate the QE.

To emphasize, in the same field of endeavor, quantization and compression/reordering of image data, Zlotnick teaches of using quantized images and reordering pixels by value and location and discloses this step in Figure 2. Furthermore, he discloses the absolute difference in position of the pixels values of neighboring pixels is used in the quantization process for rendering the image data, (Zlotnick, Column 6, Lines 1-43)

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the rendering process, as taught by Zlotnick, with Van Dalfsen's correction circuit, as modified by Kwak, with the motivation that by quantizing properly, an efficient compression can be had, reducing the size of the image data, saving space and also allowing for a sharper image, (Zlotnick, Column 1, Lines 50-56)

Van Dalfsen teaches in Claim 3:

A video circuit for processing video signals which show images on a display panel with linear light transition ([0005]), comprising a gamma correction means ([0037]), a quantization means (Figure 3, quantizer 304, [0046]) and a sub-field generation means ([0001], Figure 3, 306 and Column 3, Table 1 shows the combinations), but

Van Dalfsen does not explicitly teach that the circuit is “wherein the quantization means is a random-access memory.”

However, in the same field of endeavor, display driving methods, Kwak teaches in Figures 2 and 7 to use LUTs (read as memory) to replace the quantizer to alter the properties of the signals. (Column 9, Lines 11-16 and Column 5, Lines 21-24).

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the quanitzer as a LUT as taught by Kwak with Van Dalfsen’s display device by replacing the quantizer with a LUT with the motivation that “Larger look up tables make integration more difficult and increases system costs. In addition, a programmable system for gamma correction typically uses RAM such as SRAM or DRAM for the look up table, instead of ROM. However, RAM is typically more complicated and larger than ROM, making look up table size even more critical in programmable systems. (Kwak, Column 1, Lines 65-67) The LUT has physical advantages in terms of size and would useful to utilize as the quantization means. Furthermore, it is obvious to one of skill in the art that the respective LUTs are associated with the addition and multiplier functions.

Kwak does not explicitly teach “wherein multiple quantization errors of different neighboring pixels of a current pixel are used to quantize the current pixel.” As discussed above, he does teach of making adjustments/quantizing the data as discussed above.

However, using absolute values in comparing the neighboring pixel data to determine the quantization error, QE, of the current pixel, is well known in the art and is commonly used to calculate the QE.

To emphasize, in the same field of endeavor, quantization and compression/reordering of image data, Zlotnick teaches of using quantized images and reordering pixels by value and location and discloses this step in Figure 2. Furthermore, he discloses the absolute difference in position of the pixels values of neighboring pixels is used in the quantization process for rendering the image data, (Zlotnick, Column 6, Lines 1-43).

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the rendering process, as taught by Zlotnick, with Van Dalfsen's correction circuit, as modified by Kwak, with the motivation that by quantizing properly, an efficient compression can be had, reducing the size of the image data, saving space and also allowing for a sharper image, (Zlotnick, Column 1, Lines 50-56)

As per Claim 5:

A video circuit (Van Dalfsen, [0005]) as claimed in claim 3, but

Van Dalfsen does not explicitly teach that the circuit is “wherein the random-access memory is said gamma correction means.”

However, in the same field of endeavor, display driving methods, Kwak teaches “A conventional gamma correction apparatus uses a look up table stored in a memory such as a RAM or ROM.” (Column 1, Lines 48-50). The RAM is used to assist in the process, to the point where it considered to be the gamma correction means.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the gamma correction circuit as a RAM as taught by Kwak with Van Dalfsen’s display device with the motivation that “Larger look up tables make integration more difficult and increases system costs. In addition, a programmable system for gamma correction typically uses RAM such as SRAM or DRAM for the look up table, instead of ROM. However, RAM is typically more complicated and larger than ROM, making look up table size even more critical in programmable systems. (Column 1, Lines 65-67) The LUT has physical advantages in terms of size.

Van Dalfsen teaches in Claim 7:

A video circuit as claimed in claim 3, wherein the random-access memory is said sub-field generation means. (Figure 3, [0046], “The image display unit has a look up table 306

containing the available levels and specifying what combinations of the ten available sub-fields are to be used for the respective levels." As interpreted, the random-access memory provides for subfield generation means.)

9. **Claims 4 and 6** rejected under 35 U.S.C. 103(a) as being unpatentable over Van Dalfsen et al. (US 2001/0005186 A1), Kwak et al. (6,166,781) and Zlotnick (US 6,522,784 B1) as applied to claim 3, above, and further in view of Okada et al. (US 5,854,799)

As per Claim 4:

A video circuit (Van Dalfsen, [0005]) as claimed in claim 3, but

Van Dalfsen and Kwak do not explicitly teach that the circuit is "wherein the random-access memory additionally performs dequantization"

However, in the same field of endeavor, display driving methods, Okada teaches "The dequantizer 107 performs dequantization on the variable-length decoded data based on quantization threshold values stored in a quantization table, stored in the second ROM 111, to attain DCT (Discrete Cosine Transform) coefficients. (Okada, Column 3, Lines 8-12). The memory provides for dequantization means.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the dequantizer as a memory as taught by Okada with Van Dalfsen's

display device by implementing the dequantizer after the gamma correction circuit and quantizer with the motivation that “Based upon the dequantized data, a direct current error detector checks macroblocks by macroblock to determine if an erroneous macroblock exists. Each slice of a picture is checked. If an erroneous macroblock is found, an error processing circuit replaces the erroneous macroblock with a corresponding macroblock from a preceding picture.” (Okada, Columns 3-4, Lines 66-4) By using the dequantizer, it can be determined if an error was made and can subsequently be removed.

Van Dalfsen and Okada teach in Claim 6:

A video circuit as claimed in claim 4, wherein an inverse gamma circuit is arranged downstream of the random access memory. (The quanitzer will alter the signals determined from the gamma correction curve and the dequantizer as taught by Okada will adjust the signals in the quantizer.)

10. **Claims 8-11** rejected under 35 U.S.C. 103(a) as being unpatentable over Van Dalfsen et al. (US 2001/0005186 A1) and Kwak et al. (6,166,781) and Zlotnick (US 6,522,784 B1) as applied to claim 3, above, and further in view of Lengyel (US 6,614,428 B1)

Van Dalfsen teaches in Claim 8:

A video circuit ([0005]) as claimed in claim 7, wherein sub-field generation ([0046]) values are applied to a filter ([0046], “error filter 312”) via a conversion means ([0046],

"addressing unit 308. This unit controls the switching of the cell during the various sub-fields when displaying image."), but

Van Dalfsen and Kwak do not explicitly teach that the circuit has a "dequantization means"

However, in the same field of endeavor, image display, Lengyel teaches "Dequantizer 222 reconstructs the basis coefficients and dequantizer 224 reconstructs the residual." (Column 19, Lines 42-45) Dequantizer 222 is used to convert the altered signal back to the original form.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the dequantizer as taught by Lengyel with Van Dalfsen's display device by implementing the dequantizer after the gamma correction circuit and quantizer with the motivation that "The residual in this case measures the distortion between the transformed base rigid body and the current mesh" (Column 9, Lines 62-64) and "The compressor quantizes and encodes the transformation parameters of the geometric transforms, the base mesh, and residuals. To minimize the distortion of the reconstructed meshes in the decompressor, the compressor computes the residual using quantized/de-quantized transformation and base mesh parameters." (Column 10, Lines 46-50) In order to minimize distortion, the quantized/de-quantized method is used to eliminate the residual.

Van Dalfsen teaches in Claim 9:

A video circuit ([0005]) as claimed in claim 8, wherein the filter applies values to an adder which is situated in an input area of a second signal which represents pixel values of a neighboring line. ([0046], "The difference between the two values, which is the error originating from the quantization, is fed to error filter 312. The output of the filter is added to the value of one or more following pixels, depending on the nature of the filter, by adder 314." The output after the adder represents the pixel value of the neighboring pixel line.)

Van Dalfsen and Lengyel teach in Claim 10:

A video circuit ([0005]) as claimed in claim 7, wherein the sub-field generation means values are applied to the adder via a second conversion means (Van Dalfsen, [0046], "addressing unit 308. This unit controls the switching of the cell during the various sub-fields when displaying image.") and a second dequantizion means. (Lengyel, Column 19, Lines 42-45, The second dequantizer 224. The combination teaches to use the dequantizion means.)

Van Dalfsen and Kwak teach in Claim 11:

A video circuit ([0005]) as claimed in claim 9, wherein pixel values of the neighboring line are quantized in a further quantization means and sub-fields are generated in a further sub-field generation means (A sub-field generator uses the most significant bits to determine the values in the next sub-field and these bits are quantized in the LUTs), wherein a further random access memory is said further quantization means and said further sub-field generation means. (The combination teaches to use the quantization and sub-field generation means.)

11. **Claims 13-15 and 18** rejected under 35 U.S.C. 103(a) as being unpatentable over Van Dalfsen et al. (US 2001/0005186 A1) in view of Kwak et al. (6,166,781), Zlotnick (US 6,522,784 B1) in view of Adachi et al. (US 2004/0081266 A1)

As per Claims 13-15:

The cited references do not explicitly teach of a quantization process using multiplier elements, adders and delay elements.

However, these are well known elements in the art that are used in the quantization process.

To emphasize, in the same field of endeavor, quantization, Adachi teaches and shows in Figure 14 of using adders 208 and 240, multipliers 211 and delay circuits 209, used in conjunction with quantizer 202, (Adachi, Figure 14, [0206]).

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use the quantizing circuit, as taught by Adachi, with the motivation that it is a well known structure in the art and that by doing so, a better signal with a lower spurious level can be achieved, (Adachi, [0018]).

Adachi teaches in Claim 16:

A video circuit as claimed in claim 13 further comprising memory configured to store a constant value, wherein the adder is further configured to add the processing result, the constant

value and the current pixel to generate the combined result. **(Please note that a constant value is a vague, indefinite term. Figure 14 shows the adder to combined a fraction part F)**

Adachi teaches in Claim 18:

A video circuit as claimed in claim 13 further comprising a rounding circuit coupled to the adder and the quantizer, wherein the rounding circuit is configured to perform a rounding function on the combined result to generate a rounded result, wherein the quantizer quantizes the current pixel using the rounded result. **(Please notes Figures 14 and 19, fraction part F, [0030] and [0136])**

Response to Applicant's Arguments

12. Applicant's arguments considered, but are respectfully moot in grounds of new rejection(s).

112 rejections have been given for some of the new claimed matter and Applicant is respectfully asked to clarify the issues, thank you.

As for Applicant's arguments on Claims 1-3, these are respectfully not persuasive. The LUTs are mentioned several times in Kwak as being tied to the respective adder and multiplier processes. One of ordinary skill in the art would certainly realize this and see what the purpose of the LUTs are for.

Applicant has added more claims and the Adachi reference has been added to teach of the well known components that are used in the quantization process. Examiner further asserts

Official Notice and will provide additional references to back up the statement that it is well known, if Applicant requests them.

Applicant is advised to clear up the 112 issues with the allowable subject matter or perhaps claim the quantization curves as shown in Figures 9 and 10 to overcome the current rejection.

Conclusions

Applicant's amendments and non-persuasive arguments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629